



8-Channel Latchable Multiplexers

DG528/DG529

General Description

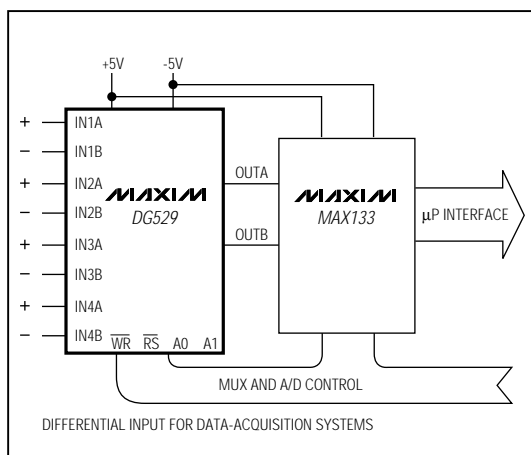
Maxim's DG528/DG529 are monolithic, 8-channel, CMOS multiplexers with on-board address and control latches that simplify design and reduce board space in microprocessor-based applications. The DG528 is a single-ended, 1-of-8 multiplexer, while the DG529 is a differential, 2-of-8 multiplexer. These devices can operate as multiplexers or demultiplexers.

The DG528/DG529 have break-before-make switching to prevent momentary shorting of the input signals. Each device operates with dual supplies ($\pm 4.5\text{V}$ to $\pm 20\text{V}$) or a single supply ($+5\text{V}$ to $+30\text{V}$). All logic inputs are TTL and CMOS compatible. The Maxim DG528/DG529 are pin and electrically compatible with the industry-standard DG528/DG529.

Applications

- Data-Acquisition Systems
- Automatic Test Equipment
- Avionics and Military Systems
- Communication Systems
- Microprocessor-Controlled Systems
- Audio-Signal Multiplexing

Typical Operating Circuit



Features

- ◆ Low-Power, Monolithic CMOS Design
- ◆ On-Board Address Latches
- ◆ Break-Before-Make Input Switches
- ◆ TTL and CMOS Logic Compatible
- ◆ Microprocessor-Bus Compatible
- ◆ $r_{DS(ON)} < 400\Omega$
- ◆ Pin and Electrically Compatible with the Industry-Standard DG528/DG529 and ADG528/ADG529

Ordering Information

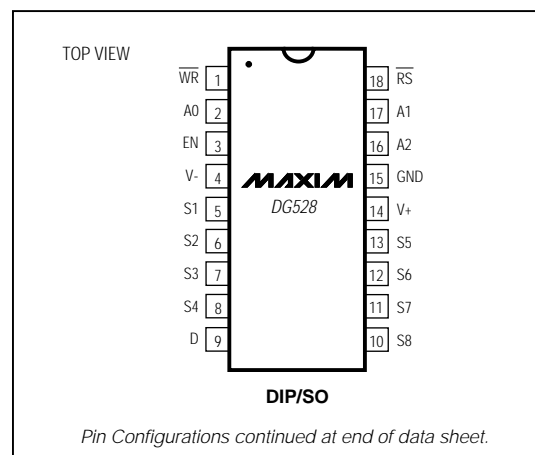
PART	TEMP. RANGE	PIN-PACKAGE
DG528CJ	0°C to +70°C	18 Plastic DIP
DG528CWN	0°C to +70°C	18 Wide SO
DG528CK	0°C to +70°C	18 CERDIP
DG528C/D	0°C to +70°C	Dice*
DG528DJ	-40°C to +85°C	18 Plastic DIP
DG528DN	-40°C to +85°C	20 PLCC
DG528EWN	-40°C to +85°C	18 Wide SO
DG528DK	-40°C to +85°C	18 CERDIP
DG528AZ	-55°C to +125°C	20 LCC**
DG528AK	-55°C to +125°C	18 CERDIP**

Ordering Information continued at end of data sheet.

* Contact factory for dice specifications.

** Contact factory for availability and processing to MIL-STD-883.

Pin Configurations



Pin Configurations continued at end of data sheet.



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DG528/DG529

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-	18-Pin Wide SO (derate 9.52mW/°C above +70°C)762mW
V++44V	18-Pin CERDIP (derate 10.53mW/°C above +70°C)....842mW
GND+25V	20-Pin PLCC (derate 10.00mW/°C above +70°C)800mW
Digital Inputs Vs, VdV- -2V to V+ +2V	20-Pin LCC (derate 9.09mW/°C above +70°C)727mW
or 20mA, whichever occurs first.	Operating Temperature Ranges
Current (any terminal, except S or D)30mA	DG52_C_0°C to +70°C
Continuous Current, S or D	DG52_D_/E_-40°C to +85°C
Peak Current, S or D20mA	DG52_A_-55°C to +125°C
(pulsed at 1ms, 10% duty cycle max)50mA	Storage Temperature Range-65°C to +150°C
Continuous Power Dissipation (TA = +70°C) (Note 1)	Lead Temperature (soldering, 10sec)+300°C
18-Pin Plastic DIP (derate 11.11mW/°C above +70°C) ...889mW	

Note 1: All leads are soldered or welded to PC board.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 15V, V- = -15V, VEN = 2.4V, WR = 0V, RS = 2.4V, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	DG52_A			DG52_C/D/E			UNITS			
			MIN	TYP	MAX	MIN	TYP	MAX				
SWITCH												
Analog-Signal Range	VANALOG	(Note 2)	-15		15	-15		15	V			
Drain-Source On-Resistance	rDS(ON)	VD = ±10V, VAL = 0.8V, IS = -200µA, VAH = 2.4 (Note 3)	TA = +25°C, TMIN		270	400	270		450	Ω		
			TA = TMAX		500		500					
Greatest Change in Drain-Source On-Resistance Between Channels	ΔrDS(ON)	-10V < VS < 10V	TA = +25°C		6		6		%			
Source-Off Leakage Current	IS(OFF)	VEN = 0V, VS = ±10V, VD = ±10V	TA = +25°C		-1	-0.005	1	-5	-0.005	5	nA	
			TA = TMAX		-50	-0.005	50	-50	-0.005	50		
Drain-Off Leakage Current	ID(OFF)	VEN = 0V, VS = ±10V, VD = ±10V	DG528	TA = +25°C		-10	-0.015	10	-20	-0.015	20	nA
				TA = TMAX		-200	-0.015	200	-200	-0.015	200	
			DG529	TA = +25°C		-10	-0.008	10	-20	-0.008	20	
				TA = TMAX		-100	-0.008	100	-100	-0.008	100	
Drain-On Leakage Current (Notes 3, 4)	ID(ON)	VAH = 2.4V, VS = VD = ±10V, VAL = 0.8V, VEN = 2.4V	DG528	TA = +25°C		-10	-0.03	10	-20	-0.03	20	nA
				TA = TMAX		-200	-0.03	200	-200	-0.03	200	
			DG529	TA = +25°C		-10	-0.015	10	-20	-0.015	20	
				TA = TMAX		-100	-0.015	100	-100	-0.015	100	
INPUT												
Address Input Current, Input Voltage High	IAH	VA = 2.4V	TA = +25°C		-1	-0.002	1	-1	-0.002	1	µA	
			TA = TMAX		-30		-30					
		VA = 15V	TA = +25°C		-1	-0.006	1	-1	-0.006	1		
			TA = TMAX		30		30					
Address Input Current, Input Voltage Low	I _{AL}	VA = RS = WR = 0V, VEN = 0V or 2.4V	TA = +25°C		-1	-0.002	1	-1	-0.002	1	µA	
			TA = TMAX		-30	-0.01		-30	-0.01			

8-Channel Latchable Multiplexers

DG528/DG529

ELECTRICAL CHARACTERISTICS

(V₊ = 15V, V₋ = -15V, V_{EN} = 2.4V, \overline{WR} = 0V, \overline{RS} = 2.4V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	DG52_A			DG52_C/D/E			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC									
Switching Time of Multiplexer	t _{TRANS}	Figure 1	T _A = +25°C		0.4	1	1.5		μs
Break-Before-Make Interval	t _{OPEN}	Figure 2	T _A = +25°C		0.2		0.2		μs
Enable, Write Turn-On Time	t _{ON(EN, \overline{WR})}	Figures 3, 4	T _A = +25°C		1.0	1.5	1.5		μs
Enable, Reset Turn-Off Time	t _{OFF(EN, \overline{RS})}	Figures 3, 5	T _A = +25°C		0.4	1	1.5		μs
Charge Injection	Q	Figure 6	T _A = +25°C		4		4		pC
Off Isolation	O _{IRR}	V _{EN} = 0V, R _L = 1kΩ, C _L = 15pF, V _S = 7V _{RMS} , f = 500kHz	T _A = +25°C		68		68		dB
Logic-Input Capacitance	C _{IN}	f = 1MHz	T _A = +25°C		2.5		2.5		pF
Source-Off Capacitance	C _{S(OFF)}	V _{EN} = 0V, f = 140kHz, V _S = 0V	T _A = +25°C		5		5		pF
Drain-Off Capacitance	C _{D(OFF)}	V _{EN} = 0V, f = 140kHz, V _S = 0V	DG528	T _A = +25°C	25		25		pF
			DG529	T _A = +25°C	12		12		
SUPPLY									
Positive Supply Current	I ₊	V _{EN} = V _{AH} = 0V	T _A = +25°C		0.003	2.5	0.003	2.5	mA
Negative Supply Current	I ₋	V _{EN} = V _{AH} = 0V	T _A = +25°C		-1.5	0.01	-1.5	0.01	mA
MINIMUM INPUT TIMING									
\overline{WR} Pulse Width	t _{WW}	Figure 7			300	150	300	15	ns
AX, EN Data Valid to \overline{WR}	t _{DW}	(Stabilization Time) Figure 7			180	120	180	12	ns
AX, EN Data Valid after \overline{WR}	t _{WD}	(Hold Time) Figure 7			30	10	30	10	ns
\overline{RS} Pulse Width	t _{RS}	Figure 7; V _S = 5V (Note 5)			500	150	500	150	ns

Note 2: Guaranteed by design.

Note 3: Sequence each switch on.

Note 4: I_{D(ON)} is leakage from driver into on switch.

Note 5: Reset pulse period must be at least 50μs during or after power-on.

8-Channel Latchable Multiplexers

DG528/DG529

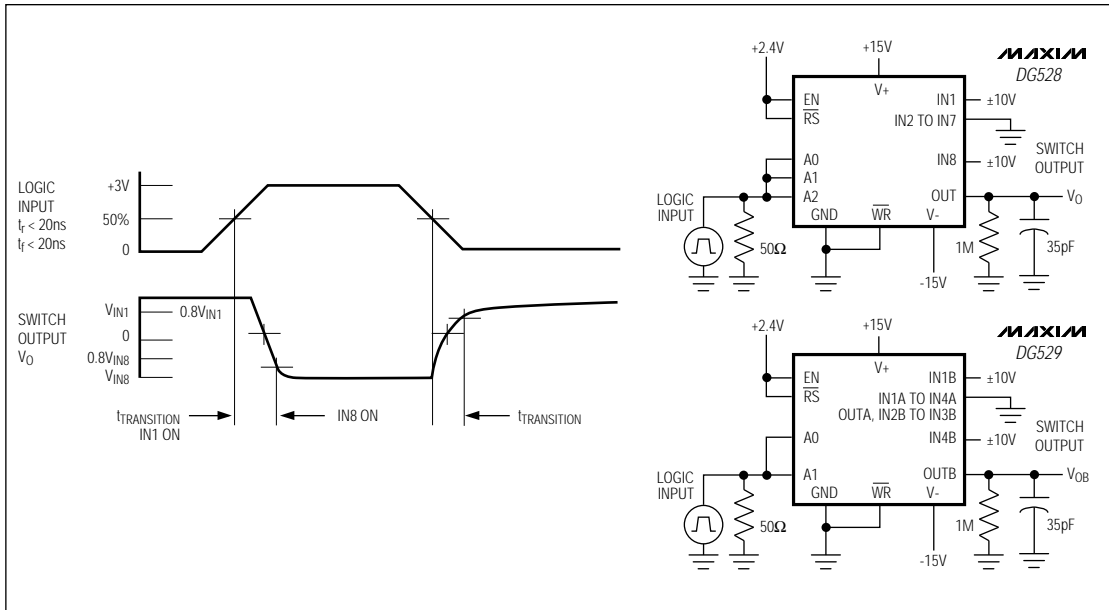


Figure 1. Transition-Time Test Circuits

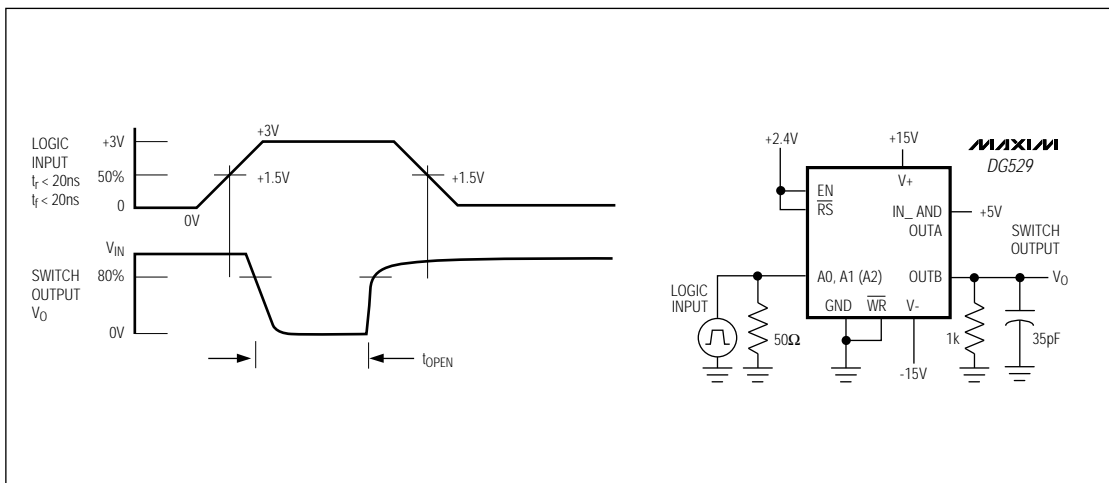


Figure 2. Open-Time (B.B.M.) Interval Test Circuit

8-Channel Latchable Multiplexers

DG528/DG529



Figure 3. Enable t_{ON}/t_{OFF} Time Test Circuit



Figure 4. Write Turn-On Time $t_{ON}(\overline{WR})$ Test Circuit

8-Channel Latchable Multiplexers



Figure 5. Reset Turn-Off Time $t_{OFF}(\overline{RS})$ Test Circuit

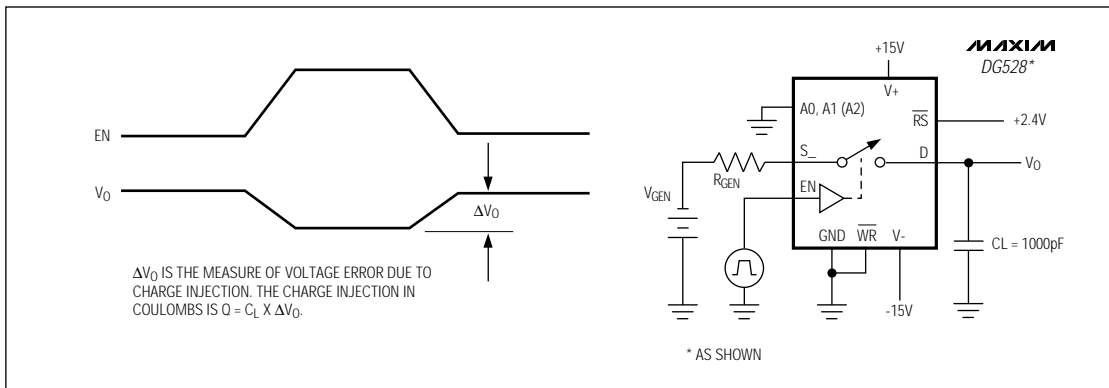


Figure 6. Charge-Injection Test Circuit

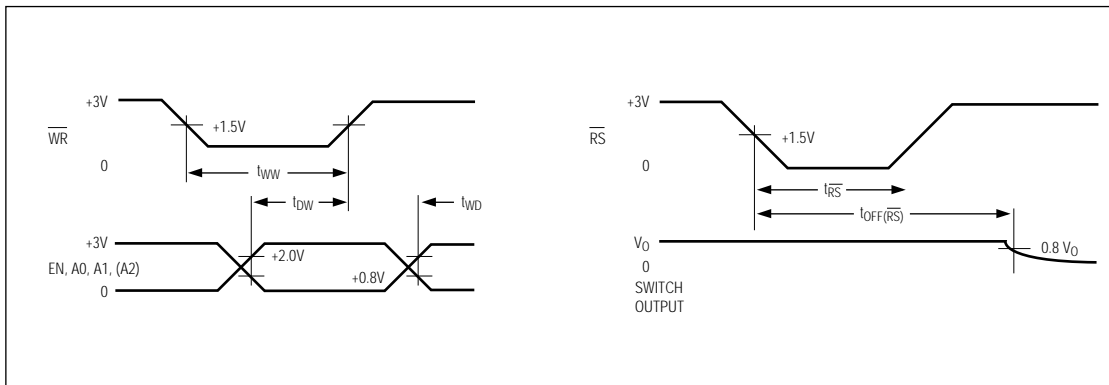


Figure 7. Typical Timing Diagrams for DG528/DG529

8-Channel Latchable Multiplexers

DG528/DG529

Table 1. DG528 Logic States

A2	A1	A0	EN	\overline{WR}	\overline{RS}	ON SWITCH
Latching						
X	X	X	X	\downarrow	1	Maintains previous switch condition
Reset						
X	X	X	X	X	0	None (latches cleared)
Transparent Operation						
X	X	X	0	0	1	None
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

Table 2. DG529 Logic States

A1	A0	EN	\overline{WR}	\overline{RS}	ON SWITCH
Latching					
X	X	X	\downarrow	1	Maintains previous switch condition
Reset					
X	X	X	X	0	None (latches cleared)
Transparent Operation					
X	X	0	0	1	None
0	0	1	0	1	1
0	1	1	0	1	2
1	0	1	0	1	3
1	1	1	0	1	4

Note: Logic "1": $V_{AH} \geq 2.4V$, Logic "0": $V_{AL} \leq 0.8V$.

Detailed Description

The internal structures of the DG528/DG529 include translators for the A2/A1/A0/EN/ \overline{WR} / \overline{RS} digital inputs, latches, and a decode section for channel selection (Truth Tables). The gate structures consist of parallel combinations of N and P MOSFETs.

\overline{WRITE} (\overline{WR}) and \overline{RESET} (\overline{RS}) strobes are provided for interfacing with μP -bus lines (Figure 9), alleviating the need for the μP to provide constant address inputs to the mux to hold a particular channel.

When the \overline{WR} strobe is in the low state (less than 0.8V) and the \overline{RS} strobe is in the high state (greater than 2.4V), the muxes are in the transparent mode—they act similarly to nonlatching devices, such as the DG508A/DG509A or the HI508/HI509.

When the \overline{WR} goes high, the previous BCD address input is latched and held in that state indefinitely. To pull the mux out of this state, either \overline{WR} must be taken

low to the transition state, or \overline{RS} must be taken low to turn off all channels.

\overline{RS} turns off all channels when it is low, which resets channel selection to the channel 1 mode.

The DG528/DG529 work with both single and dual supplies and function over the +5V to +30V single-supply range. For example, with a single +15V power supply, analog signals in the 0V to +15V range can be switched normally. If negative signals around 0V are expected, a negative supply is needed. However, only -5V is needed to normally switch signals in the -5V to +15V range (-5V, +15V supplies). No current is drawn from the negative supply, so Maxim's MAX635 DC-DC converter is an ideal choice.

The EN latch allows all switches to be turned off under program control. This is useful when two or more DG528s are cascaded to build 16-line and larger analog-signal multiplexers.

8-Channel Latchable Multiplexers



Figure 8. Simplified Internal Structure

Applications

Operation with Supply Voltages Other Than $\pm 15\text{V}$

Maxim guarantees the DG528/DG529 for operation from $\pm 4.5\text{V}$ to $\pm 20\text{V}$ supplies. The switching delays increase by about a factor of two at $\pm 5\text{V}$, and break-before-make action is preserved.

The DG528/DG529 can operate with a single $+5\text{V}$ to $+30\text{V}$ supply as well as asymmetrical power supplies like $+15\text{V}$ and -5V . The digital threshold will remain approximately 1.6V above the GND pin, and the analog characteristics such as $r_{DS(ON)}$ are determined by the total voltage difference between V_+ and V_- . Connect V_- to 0V when operating with a $+5\text{V}$ to $+30\text{V}$ single supply.

Digital Interface Levels

The typical digital threshold of both the address lines and EN is 1.6V with a temperature coefficient of approximately $-3\text{mV}/^\circ\text{C}$, ensuring compatibility with TTL logic over the temperature range. The digital threshold is relatively independent of the power-supply voltages, going from a typical 1.6V when V_+ is 15V to 1.5V typical with $V_+ = 5\text{V}$. Therefore, Maxim's DG528/DG529 operate with standard TTL logic levels, even with $\pm 5\text{V}$ power supplies. In all cases, EN's threshold is the same as the other logic inputs and is referenced to GND.

The digital inputs can also be driven with CMOS logic levels swinging from either V_+ to V_- or from V_+ to GND. The digital input current is just a few nanoamps of leakage at all input-voltage levels with a guaranteed maximum of $1\mu\text{A}$. The digital inputs are protected from ESD by a 30V zener diode between the input and V_+ and can be driven $\pm 2\text{V}$ beyond the supplies without drawing excessive current.

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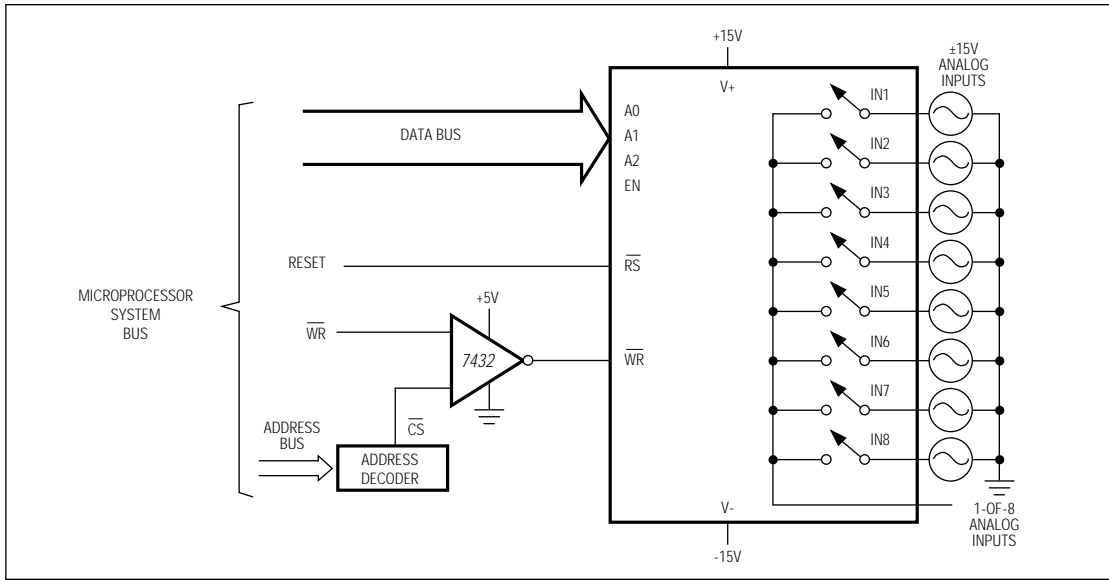
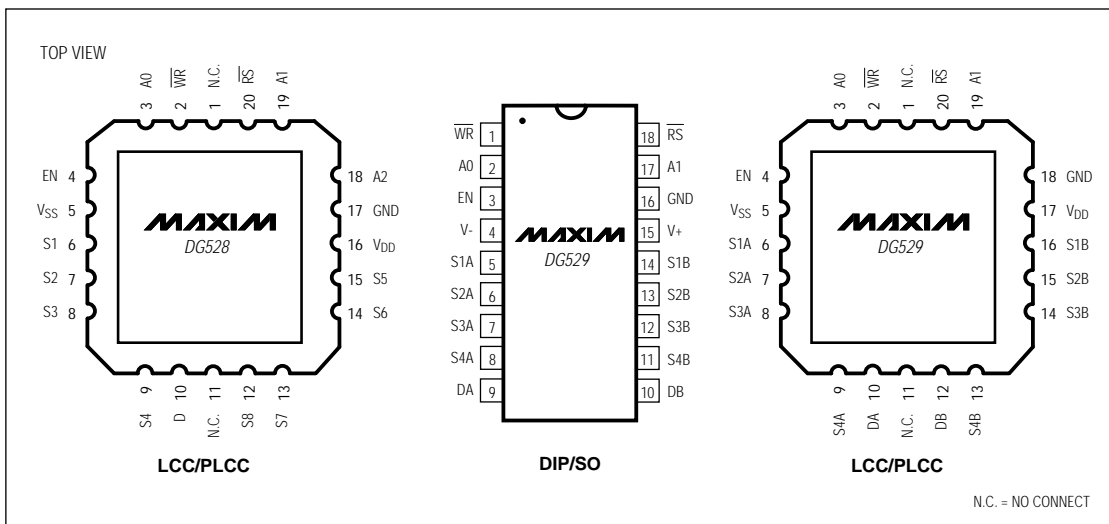


Figure 9. Bus Interface

Pin Configurations (continued)



8-Channel Latchable Multiplexers

DG528/DG529

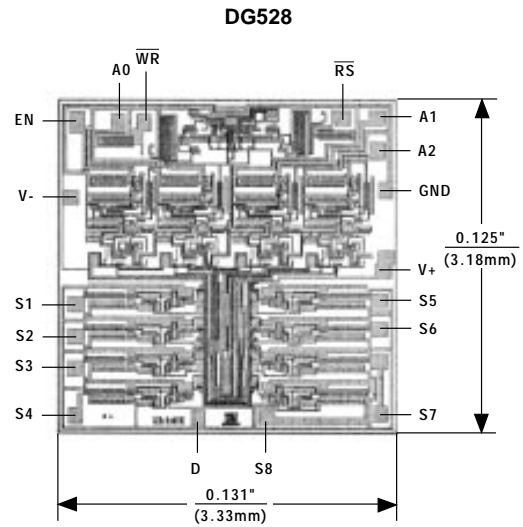
_Ordering Information (continued)

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DG529DK	-40°C to +85°C	18 CERDIP
DG529AZ	-55°C to +125°C	20 LCC**
DG529AK	-55°C to +125°C	18 CERDIP**

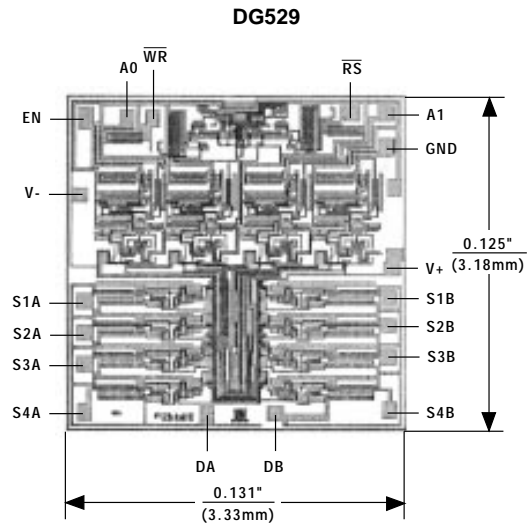
* Contact factory for dice specifications.

** Contact factory for availability and processing to MIL-STD-883.

Chip Topographies



TRANSISTOR COUNT: 200
SUBSTRATE CONNECTED TO V+



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SUBSTRATE CONNECTED TO V+

8-Channel Latchable Multiplexers

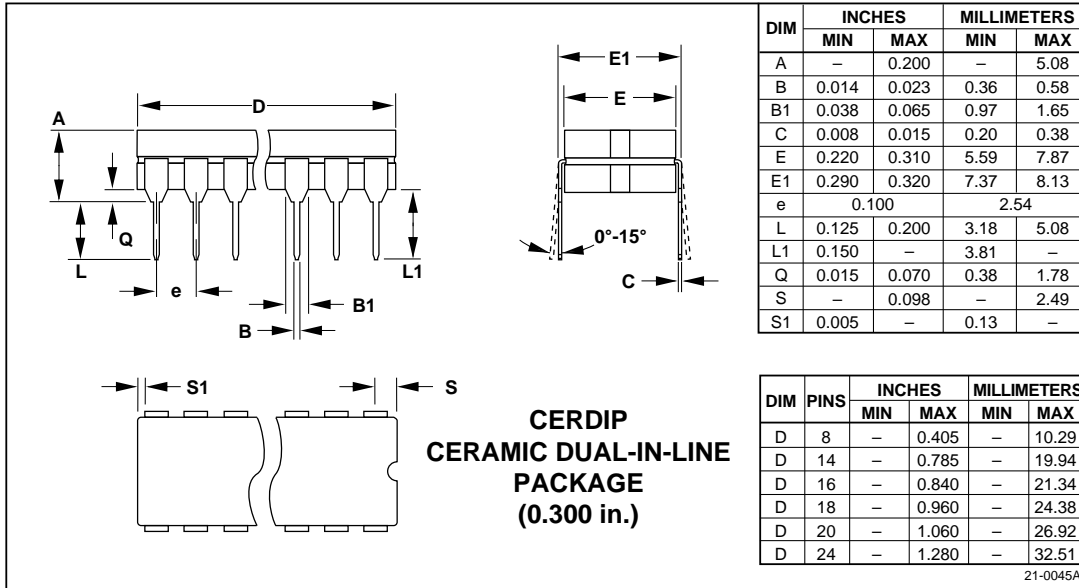
Package Information

DG528/DG529



8-Channel Latchable Multiplexers

Package Information (continued)



Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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