NEC Electronics Inc.

Preliminary

CB-C8VX/VM 3-Volt, 0.5-Micron Cell-Based CMOS ASIC

April 1996

Description

NEC's CB-C8VX/VM CMOS cell-based ASIC family facilitates the design of complete cell-based silicon systems composed of user-defined logic, complex macrofunctions such as microprocessors, intelligent peripherals, analog functions, and compiled memory blocks.

The CB-C8VX cell-based ASIC series employs a 0.5-micron (0.35-micron effective) silicon gate CMOS process with silicidation. This advanced process greatly reduces the number of contacts per cell, leading to area-efficient library elements optimized on speed with a 3.3-volt power supply. CB-C8VM, a derivative of CB-C8VX, features a unique I/O structure that provides a full 5-volt CMOS interface. For both technologies, the Titanium-Silicide process results in overall reduced power consumption per cell. Combining very high integration, high speed, and low power consumption, this technology meets today's rigorous application demands.

Fully supported by NEC's sophisticated OpenCAD® design framework, CB-C8VX/VM maximizes design quality and flexibility while minimizing ASIC design time. NEC's OpenCAD system combines popular third-party design tools with proprietary NEC tools, including advanced floorplanner and clock tree synthesis tools.

Figure 1. BGA Package Examples

Full 5-Volt CMOS Interface

CB-C8VM offers a full voltage swing interface to a 5-volt CMOS signal environment. This option is realized by implementing a section of thicker gate oxide into the I/O buffer to guarantee the necessary breakdown voltages. The 5-volt I/O buffers can be placed at any location of the I/O area and are freely mixable with 3.3-volt buffers. The internal core is identical to CB-C8VX.

Table 1. CB-C8VX/VM Series Features and Benefits

CB-C8VX/VM Series Features	CB-C8VX/VM Series Benefits
• 0.5-micron (drawn), Ti-Silicide CMOS technology	• High-density cell structure
• True 3.3 V process	• High speed at low power supply
• 36 base sizes, each with 2- and 3-metal layer options	• Flexible base sizes to best fit design needs
• Usable gates from 14K to 703K gates	• High integration capabilities
• True 5 V CMOS interface by multi-oxide I/O structure	• Supports flexible interfacing to different signal voltages
• Staggered pad ring for high gate-to-pad ratio	• Minimizes device cost for high I/O requirement
• 5 V and 3.3 V PCI buffer, including 66-MHz PCI	• Full PCI support compliant with latest PCI specification
• GTL and HSTL buffer in development	• High-speed I/F to memory and processor buses
• Low power dissipation: 1.04 mW/MHz/gate (3.3 V)	• Ideally-suited for hand-held applications
• Extensive macro range (CPUs, peripherals, analog)	• Advanced system-on-silicon capabilities
• Memory compiler for various types of memory blocks	• Area-effective memory integration on chip
• Extensive package support: PQFP, TQFP, BGA, TBGA	• Delivers the latest package requirements
• Automatic clock skew control by clock tree synthesis	• Minimizes on-chip clock skew
• OpenCAD: popular, third-party CAE tools supported	• Smooth design flow from customer design to silicon

5-Volt-Tolerant Interface

CB-C8VX supports both 3.3-volt and 5-volt-tolerant signaling. The 5-volt-tolerant buffers enable CB-C8VX devices to communicate with 5-volt TTL signals while protecting the ASIC. CB-C8VX requires only a 3.3-volt power supply.

Integration and Performance

Gate complexities up to 703K usable gates can be integrated on the largest of 36 die sizes, each routable with 2- or 3-metal layers. This gives enough flexibility to optimally fit design needs. Twenty-two die sizes offer a single I/O pad ring and 14 are equipped with a staggered dual pad ring in order to achieve a high pad-to-gate ratio. For details, please refer to Table 2 and Table 3.

The family offers an extensive library of primitive macrofunctions characterized for 3.3-volt operation. Each of these blocks has several different drive strengths, allowing the synthesis tool to select the most suitable block for the required internal load. This generally reduces the design overhead without influencing design performance. The internal gate delay for a two-input NAND gate is 110 picoseconds (ps), (F/O=1, L=0mm) and 220 ps under loaded conditions (F/O=2, L=2mm).

To meet today's high-speed demands, high-performance I/O macros are mandatory. CB-C8VX/VM supports macros such as GTL and HSTL for fast, low-power data transfer, PLLs to synchronize on-chip system clocks, and PCI signaling standards. Also, CB-C8VX/VM offers a variety of macrofunctions to be incorporated on a single chip. These macrofunctions include CPU cores, peripheral devices, RAM/ROM and analog functions, enabling designers to create systems on silicon.

Low Power Consumption

NEC's CB-C8VX/VM Ti-Silicide process features exceptionally low power dissipation to facilitate high-speed operation without the need of costly package options, and drastically increases battery life for hand-held applications. At 3.3-volts, power dissipation for internal cells is 1.04 µW/gate/MHz.

Table 2. CB-C8VX/VM Die Steps **(124µ pad pitch)**

Step	I/O	Max. Usable Gates(1)	
		2 Layer	3 Layer
B18	88	13078	19617
B57	104	18797	28195
B97	120	25438	38156
C37	136	33219	49828
C76	152	42016	63023
D16	168	51703	77555
D55	184	62547	93820
D75	192	67969	101953
E15	208	80484	120727
E54	224	93875	140813
E94	240	106000	159000
F34	256	120969	181453
F74	272	136641	204961
G14	288	153500	230250
G53	304	171234	256852
G93	320	183078	274617
H33	336	202328	303492
H72	352	222219	333328
J32	376	254094	381141
J71	392	275813	413719
K11	408	298797	448195
K90	440	347031	520547

Single pad ring die steps.
(1) Glue logic only, with average utilization.

Table 3. CB-C8VX/VM Die Steps
(80µ staggered pad pitch)

Step	I/O	Max. Usable Gates(1)	
		2 Layer	3 Layer
B73T	148	18844	28266
C37T	188	30250	45375
C50T	196	32703	49055
D01T	228	44000	66000
D52T	260	57047	85570
D90T	284	67797	101695
E54T	324	88281	132422
F18T	364	109125	163688
F70T	396	128875	193313
G34T	436	155297	232945
H49T	508	202766	304148
J51T	572	256047	384070
K92T	660	337531	506297
M97T	788	468984	703477

Dual pad ring die steps.
(1) Glue logic only, with average utilization.

Multi-Voltage I/O Interface

For those systems not yet ready to migrate completely to 3.3-volts, CB-C8 has a full 5-volt CMOS interface available. Applying two additional process steps that realize a "multi-oxide" section in the I/O area, 5-volt speed and drive capabilities are available with the help of a separate 5-volt supply rail. The 5-volt I/O buffers include level shifters to convert the 5-volt signal levels to the internal core supply voltage of 3.3-volts. This CB-C8 derivative is called CB-C8VM and is, except for the different I/O structure, identical to CB-C8VX.

For moderate speed and driveable 5-volt I/O cell requirements, CB-C8VM's flexibility provides tolerant I/Os that safely interface to 5V devices using a single 3.3-volt power supply.

In both cases, the 3.3-volt and 5-volt interfaces can be mixed without restriction along the entire I/O ring.

	CB-C8VX	CB-C8VM
Device Names	µPD97xxx	µPD99xxx
Interface options	• true 3.3 V • 5 V tolerant	• true 3.3 V • 5 V tolerant • true 5 V CMOS
Core voltage	3.3 V	3.3 V
I/O voltage	3.3 V	3.3 V and 5 V

System on Silicon

NEC offers a wide selection of CPU/MCU cores, industry-standard intelligent peripheral macros, and compilable RAM/ROM blocks as well as analog functions in hard macro form that can be integrated onto a single CB-C8VX/VM chip. Including such macrofunctions in an ASIC design makes it possible to achieve a high level of integration, performance, and system security.

The range of NEC's on-chip macrofunctions includes NEC's proprietary 32-bit V810™ RISC CPU, and an upgraded high-speed version of the popular 16-bit CPU V30HL™, called V30MX™, which operates at clock speeds of 33 MHz at 3.3-volts, and offers an improved 286-compatible address pipelining and uses a 24-bit address bus. Other specific cores can be implemented on request. For details about the full range of on-chip macrofunctions, refer to Table 4.

Embedded macrofunctions are easy to place, route, and simulate. Because these macros are derived from NEC's standard parts, they have fully characterized parameters and can be tested with standard test vectors to ensure full functionality and reliability.

NEC's test bus architecture allows complete system simulation, production testing of the internal circuits of the macrofunctions, and seamless embedded CPU core emulation. The CPU may be connected externally and can be replaced by an in-circuit emulator (ICE). All this is performed with only two dedicated test control pins.

Table 4. Macrofunction Range

Macro	Comparable Device	Description
NZ 70008H	µPD70008A	Z80™: 8-bit microprocessor (16 MHz)
NZ V30MX	µPD70108H	V30MX: 16-bit microprocessor (16-bit data bus, 33 MHz)
NZ V810	µPD70732	V810™: 32-bit RISC microprocessor (25 MHz)
NZ 71037H	µPD71037	Programmable DMA controller (4 channels, 20 MHz)
NZ 71051H	µPD71051	USART: serial data control (full-duplex Tx/Rx, 300kbit/s, 20 MHz)
NZ 71054H	µPD71054	Programmable timer/counter (16-bit, 3 counter, 6 modes, 20 MHz)
NZ 71055H	µPD71055	Programmable parallel interface (8-bit, 3 I/O ports, 3 modes)
NZ 71059H	µPD71059	Programmable interrupt control (64 interrupt request inputs)
NA 4993	µPD4993	8-bit parallel I/O real-time clock
NA 72065BL	µPD72065B	Single-double density floppy disk controller
NZ 72103	µPD72103	HDLC Controller: Full duplex, Baud rate 4 Mbps, built-in DMA
M I^2C™	—	I^2C Bus interface: receive, transmit, master and slave
NA 16450L	NS16C450	UART: for PC-compatible serial ports
NA 16550L	NS16550A	UART with FIFO: for PC-compatible serial ports

Z80 is a trademark of Zilog, Inc.
V30HL, V30MX and v810 are trademarks of NEC Corporation
I^2C is a trademark of Philips

Memory Macros

All memory blocks in NEC's CB-C8VX/VM technology are realized as embedded hard macros and are generated by a memory compiler. To ease the task of RAM testing for the designer, NEC supplies standard test pattern sets, which help to save valuable development time. NEC offers seven different types of memory blocks, as shown in Table 5.

Packaging

NEC offers a wide variety of over 60 package types. The CB-C8VX/VM family can be packaged in NEC's most popular surface-mount and through-hole packages. These include plastic quad-flat packs (PQFPs) with up to 376 pins. The QFP range includes thin packages (TQFP, LQFP), QFPs with integrated heatspreader, and tape-automated-bonding QFPs (TAB-QFP) with up to 304 pins. Pin grid arrays (PGAs) with up to 528 pins, BGA packages with up to 672 pins, and TBGA packages with up to 696 pins can be used.

CB-C8VX/VM Applications

CB-C8VX/VM devices are targeted for 3.3-volt products in telecommunications, electronic data processing (EDP), and consumer applications. Typical telecommunications applications include cellular telephones, high-end pagers, and PCMCIA devices, as well as broad-band communication systems up to 156 Mbit/s. In the EDP segment, applications range from personal computers to high-end workstations and mainframes, multimedia platforms, graphic accelerators, personal digital assistants (PDAs), notebook and pen-based devices, hand-held data terminals, and hard disk controllers. Consumer applications include games, video cameras, portable printers, and sophisticated calculators.

Each of these applications demands the benefits of increased integration and low power consumption that only a cell-based family using an optimized 3.3-volt process technology can deliver. CB-C8VX/VM provides the flexibility needed when a 3.3-volt process is required.

Design Tool Support

The CB-C8VX/VM family is fully supported by NEC's OpenCAD Design System, a unified front-to-back-end design package that allows designers to mix and match tools from the industry's most popular third-party vendors and from NEC's offering of powerful proprietary software tools. These tools perform schematic capture, logic synthesis, floorplanning, logic and timing simulation, layout, design and circuit rule check, and memory compilations.

The company's proprietary clock tree synthesis tool automatically buffers clock lines as needed to minimize clock skew, which is essential for half-micron designs. The nonlinear delay calculator ensures timing accuracy throughout the simulation, synthesis, and silicon stages. Finally, NEC's memory compiler software enables memory block generation based on size and performance requirements.

Table 5. Memory Blocks

Macro Type	Word Range	Bit Range	Step (Word / Bit)
ROM	128 - 8192 256 - 16384 512 - 32768	4 - 64 2 - 32 1 - 16	128 / 2 256 / 1 512 / 1
Low-power RAM, single-port (asynchronous, bi-directional I/O)	64 - 512 128 - 1024 256 - 2048	1 - 32 1 - 16 1 - 8	16 / 1 32 / 1 64 / 1
Low-power RAM, single-port (synchronous, separate I/O)	64 - 512 128 - 1024 256 - 2048	1 - 32 1 - 16 1 - 8	16 / 1 32 / 1 64 / 1
High-density RAM, single-port (synchronous, separate I/O)	128 - 2048	1 - 64	16 / 1
High-speed RAM, single-port (synchronous, separate I/O)	32 - 2048	1- 32	32 / 1
Register files, dual-port	8 - 256	4 - 32	4 / 1
Register files, triple-port	8 - 256	4 - 32	4 / 1

Absolute Maximum Ratings

Power supply voltage, V_{DD}	
3.3 V supply	–0.5 to +4.6 V
5 V supply	–0.5 to +6.0 V
I/O voltage, V_I/V_O	
3.3 V interface block	–0.5 to +4.6 V and ($V_I/V_O < V_{DD}$ +0.5 V)
5 V-tolerant block	–0.5 to +6.6 V and ($V_I/V_O < V_{DD}$ +3.0 V)
5 V swing block	–0.5 to +6.0 V and ($V_I/V_O < V_{DD}$ +0.5 V)
Latch-up current, I_{LATCH}	>1 A (typ)
Operating temperature, T_{OPT}	–40 to +85°C
Storage temperature, T_{STG}	–65 to +150°C

Caution: Exposure to absolute maximum ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should not be operated outside the recommended operating conditions.

Input/Output Capacitance ($V_{DD} = V_I = 0$ V; f = 1 MHz)

Terminal	Symbol	Typ	Max	Unit
Input	C_{IN}	10	20	pF
Output	C_{OUT}	10	20	pF
I/O	$C_{I/O}$	10	20	pF

(1) Values include package pin capacitance

Power Consumption

Description	Limits	Unit
Internal gate(1)	1.04	µW/MHz
Input block	—	µW/MHz
Output block	—	µW/MHz

(1) Assumes 30% internal gate switching at one time

Caution: Exposure to absolute maximum ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should not be operated outside the recommended operating conditions.

Recommended Operating Conditions (V_{DD} = 3.3 V ± 0.165 V; V_{CC} = 5.0 V ± 0.5 V; T_J = –40 to +125°C)

		3.3 V Interface Block		5 V Tolerant Block (CB-C8VX/VM)		5 V Swing CMOS Level (CB-C8VM)		5 V Swing TTL Level (CB-C8 VM)		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
I/O power supply voltage	V_{DD}	3.0	3.6	3.0	3.6	4.5	5.5	4.75	5.25	V
Junction temperature	T_J	–40	+125	–40	+125	–40	+125	–40	+125	°C
High-level input voltage	V_{IH}	2.0	V_{DD}	2.0	5.5	0.7 V_{DD}	V_{DD}	2.0	V_{DD}	V
Low-level input voltage	V_{IL}	0	0.8	0	0.8	0	0.3 V_{DD}	0	0.8	V
Positive trigger voltage	V_P	1.2	2.4	1.2	2.4	1.8	4.0	1.2	2.4	V
Negative trigger voltage	V_N	0.6	1.8	0.6	1.8	0.6	3.1	0.6	1.8	V
Hysteresis voltage	V_H	0.3	1.5	0.3	1.5	0.3	1.5	0.3	1.5	V
Input rise/fall time	t_R, t_F	0	200	0	200	0	200	0	200	ns
Input rise/fall time, Schmitt	t_R, t_F	0	10	0	10	0	10	0	10	ms

AC Characteristics (V_{DD} = 3.3 V ± 0.3 V; T_J = –40 to +125°C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Toggle frequency	f_{TOG}		480		MHz	D-F/F; F/O = 2 mm
Delay time						
2-input NAND (F322)	t_{PD}		236		ps	F/O = 1; L = 0 mm
	t_{PD}		272		ps	F/O = 2; L = typ
Flip-flop (F661)	t_{PD}		777		ps	F/O = 1; L = 0 mm
	t_{PD}		865		ps	F/O = 2; L = typ
	t_{SETUP}		420		ps	—
	t_{HOLD}		580		ps	—
Input buffer (FI01)	t_{PD}		126		ps	F/O = 1; L = 0 mm
	t_{PD}		228		ps	F/O = 2; L = typ
Output buffer (9 mA) 3.3 V	t_{PD}		1.24		ns	C_L = 15 pF
Output buffer (9 mA) 5 V-tolerant	t_{PD}		4.262		ns	C_L = 15 pF
Output buffer (6 mA) 5 V-swing	t_{PD}		2.698		ns	C_L = 15 pF
Output rise time (9 mA)	t_R		1.88		ns	C_L = 15 pF
Output fall time (9 mA)	t_F		1.32		ns	C_L = 15 pF

DC Characteristics (V_{DD} = 3.3 V ± 0.3 V, 5 V ± 0.5 V; T_A = –40 to +125°C)

Parameters	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Static current consumption	I_L	$V_I = V_{DD}$	B18 to H33			200	µA
		or GND	H72 to K90			300	µA
Off-state output current	I_{OZ}	$V_O = V_{DD}$ or GND				±10	µA
Output short-circuit current	I_{OS}	V_O = 0V				–250	mA
Input leakage current	I_I						
Normal input		$V_I = V_{DD}$ or GND			$\pm 10^{-5}$	±10	µA
With pull-up resistor (50 ký)		V_I = GND		–10	–40	–80	µA
With pull-up resistor (5 ký)		V_I = GND		–130	–350	–640	µA
With pull-down resistor (50 ký)		$V_I = V_{DD}$		10	65	130	µA
Low-level output current	I_{OL}						
3 V interface buffer		V_{OL} = 0.4V					mA
3 mA	I_{OL}			3			mA
6 mA	I_{OL}			6			mA
9 mA	I_{OL}			9			mA
12 mA	I_{OL}			12			mA
18 mA	I_{OL}			18			mA
24 mA	I_{OL}			24			mA
5 V-tolerant buffer		V_{OL} = 0.4V					mA
1 mA	I_{OL}			1			mA
2 mA	I_{OL}			2			mA
3 mA	I_{OL}			3			mA
6 mA	I_{OL}			6			mA
9 mA	I_{OL}			9			mA
5 V swing buffer		V_{OL} = 0.4V					mA
1 mA	I_{OL}			1			mA
2 mA	I_{OL}			2			mA
3 mA	I_{OL}			3			mA
6 mA	I_{OL}			6			mA
9 mA	I_{OL}			9			mA
12 mA	I_{OL}			12			mA
18 mA	I_{OL}			18			mA
High-level output current	I_{OH}						
3 V interface buffer		V_{OH} = 2.4V					
3 mA	I_{OH}			-3			mA
6 mA	I_{OH}			-6			mA
9 mA	I_{OH}			-9			mA
12 mA	I_{OH}			-12			mA
18 mA	I_{OH}			-18			mA
24 mA	I_{OH}			-24			mA

DC Characteristics (continued) (V_{DD} = 3.3 V ± 0.3 V, 5 V ± 0.5 V; T_A = –40 to +125°C)

Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-level output current	I_{OH}					
5 V-tolerant buffer		V_{OH} = 2.4 V				
1 mA	I_{OH}		–1			mA
2 mA	I_{OH}		–2			mA
3 mA	I_{OH}		–3			mA
6 mA	I_{OH}		–6			mA
9 mA	I_{OH}		–9			mA
5 V swing buffer		V_{OH} = –0.4 V				
1 mA	I_{OH}		–1			mA
2 mA	I_{OH}		–2			mA
3 mA	I_{OH}		–3			mA
6 mA	I_{OH}		–6			mA
9 mA	I_{OH}		–9			mA
12 mA	I_{OH}		–12			mA
18 mA	I_{OH}		–18			mA
Low-level output voltage	V_{OL}	I_{OL} = 0 mA		0.1		V
3 V interface buffer	V_{OL}				0.1	V
5 V interface buffer	V_{OL}				0.1	V
5 V swing buffer	V_{OL}				0.1	V
High-level output voltage	V_{OH}	I_{OH} = 0 mA				V
3 V interface buffer	V_{OH}		V_{DD}–0.1			V
5 V interface buffer	V_{OH}		V_{DD}–0.2			V
5 V swing buffer	V_{OH}		V_{DD}–0.1			V

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Document No. A10985EU1V0DS00